REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Final Office Action of November 6, 2002 has been received and contents carefully reviewed.

Claims 1-28 are currently pending. Claims 16-28 have been allowed. Reexamination and reconsideration are respectfully requested.

The Examiner rejected claims 1, 5, 7-9, 11, 12, 14, and 15 under 35 USC 103(a) as being unpatentable over Katsuya et al. (US Patent No. 6,081,310) in view of Nakamura et al. (US Patent No. 6,124,911); and rejected claims 2-4, 6, 10, and 13 under 35 USC 103(a) as being unpatentable over Katsuya et al. (US Patent No. 6,081,310) further in view of Nakamura et al. (US Patent No. 6,124,911). Applicants respectfully traverse these rejections.

Claim 1 is allowable at least for the reason that claim 1 recites a combination of elements including dry-etching a surface of the passivation layer with a gas without using a photo mask such that the surface is embossed and has a plurality of random uneven portions; and forming a reflective electrode on the embossed surface of the passivation layer such that an exterior surface of the reflective electrode is embossed.

Claim 11 is allowable at least for the reason that claim 11 recites a combination of elements including a passivation layer on the data line, source electrode, and drain electrode, an entire surface of the passivation layer being embossed and having a plurality of random uneven portions; and an embossed reflective electrode on the passivation layer.

None of the cited references, singly or in combination, teaches or suggests at least these features of the claims.

On page 2 of the Office Action, the Examiner states that Katsuya et al. fails to teach "dry etching the insulating layer" as in claim 1. In addition, Applicants submit that Katsuya et al. fail to teach "...an entire surface of the passivation layer being embossed and having a plurality of random uneven portions; and an embossed reflective electrode" as in claim 11. The Examiner cites Nakamura et al. in an attempt to cure the deficiencies of Katsuya et al.

At column 7, lines 1-28, Nakamura et al. teaches "...a resist 13 is coated on the front surface of the resultant structure and then patterned so that an opening portion 14 corresponding to each pixel is formed (see FIG. 1E). Thereafter, the resultant structure is soaked in a NH_4F solution and wet etched...Thus, the damage layer 12 is etched out with a taper angle...The taper angle may be formed by various other methods such as sol-gel method or dry etching method." Applicants submit that a photo mask or resist 13 is used for etching the insulator in Nakamura et al., which teaches away from the present invention. "After the second inter-layer shielding film 9 is formed on the TFT 7, the second inter-layer shielding film 9 is smoothed by grinding method. An inclination layer 11 is formed by etching process so that the light reflecting surface of a pixel electrode that will be formed at a later fabrication step is inclined to a base member of an opposite substrate." Column 6, line 66 to column 7, line 4. Applicants submit that it appears that the insulator has regular even patterns. Applicants submit that Nakamura et al. fails to cure the deficiencies of Katsuya et al.

In contrast, in the present application, since the passivation layer is dry-etched without using a photo mask, the surface of the passivation layer has a plurality of random uneven portions. Neither reference teaches or suggests a surface of the passivation layer being embossed and has/having a plurality of random uneven portions as in claims 1 and 11.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness and that the rejection under 35 USC 103(a) should be withdrawn.

Moreover, claims 2-10, and 12-15 are allowable by virtue of their dependence on claims 1 and 11, which are believed to be allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at (202) 496-7371. All correspondence should be sent to the address listed below.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend claims 1 and 11 as follows:

1. (Twice Amended) A fabricating method for an array substrate of a liquid crystal display device, the method comprising:

forming a gate line including a gate electrode on a substrate;

forming a gate-insulating layer on the substrate, the gate-insulating layer covering the gate line and gate electrode;

forming an active layer on the gate-insulating layer;

forming a data line, a source electrode and a drain electrode on the active layer;

forming a passivation layer on the gate-insulating layer, the passivation layer covering the data line, source electrode and drain electrode;

dry-etching a surface of the passivation layer with a gas without using a photo mask such that the surface is embossed and has a plurality of random uneven portions; and

forming a reflective electrode on the embossed surface of the passivation layer such that an exterior surface of the reflective electrode is embossed.

11. (Twice Amended) A liquid crystal display device comprising:

upper and lower substrates with a liquid crystal layer interposed therebetween;

a gate line and a gate electrode on the lower substrate;

a gate-insulating layer on the lower substrate, the gate-insulating layer covering the gate line and gate electrode;

an active layer on the gate-insulating layer;

a source electrode and a drain electrode on the active layer;

a data line on the gate-insulating layer;

a passivation layer on the data line, source electrode, and drain electrode, an entire surface of the passivation layer being embossed and having a plurality of random uneven portions; and

an embossed reflective electrode on the passivation layer.